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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,802	01/15/2004	Dae-Woong Kang	8750-042	6500

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,802	KIM ET AL	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *1-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-29 and 31-36* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election December 28, 2004.

Election/Restrictions

Applicant's election without traverse of Group I, 22-36 in the reply filed on December 28, 2004 is acknowledged. Claims 1-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Objections

Claim 26 is objected to because of the following informalities: the last line of the claim is incomplete. The line states that "an inter-gate dielectric layer interposed between the floating gate and." For purposes of examination it is assume that the dielectric is interposed between the floating gate and the control gate. Appropriate correction is required.

Claim 30 is objected to because of the following informalities: There is insufficient antecedent basis for the limitation of "...the central region of the first active region." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 32 recites the limitation "the upper corner of the first trench region" in lines 1 through 2. There is insufficient antecedent basis for this limitation in the claim. The limitation renders the claim indefinite because it is not exactly understood how the upper corner of the first trench and low voltage gate insulation layer are formed in relation to each other. For purposes of examination, the claim will be understood to mean that the low voltage gate insulation layer is formed on an upper corner of the first trench region.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 29 and 31-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,642,105 B2)

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it

constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 29, the Kim et al. shows (fig. 3) a semiconductor device comprising: a semiconductor substrate having a low voltage region (a) and a high voltage region (b); a first trench region (307 right) formed in the low voltage region to define a first active region (1b), the first active region having a protruded edge surface (the chunk of substrate 301 that is between the two adjacent trenches 309 in active region b); a first sloped region (sides of trench) interposed between the first trench region and the first active region, the first sloped region having a first incline that is downwardly extended from the protruded edge surface of the first active region; a second trench region (307 left) formed in the high voltage region to define a second active region (1a), the second active region having a relatively flat top surface; a second sloped region interposed between the second active region and the second trench region, the second sloped region (sides of trench) having a second incline that is downwardly extended from the edge corner of the first active region; a first isolation layer filling (309 right) the first trench region and covering the first incline; a second isolation layer (309 left) filling the second trench region and covering the second incline; a low voltage gate insulation layer (305b) formed on the first active region, the low voltage gate insulation layer having a top surface lower than a top surface of the first isolation layer; a high voltage

gate insulation layer (305a) formed on the second active region, the high voltage gate insulation layer having a flat top surface lower than a top surface of the second isolation layer and being thicker than the low voltage gate insulation layer, the top surfaces of the low voltage gate insulation layer and the high voltage gate insulation layer having a profile without any recessed regions.

In re claim 31, Kim shows (fig. 32) that a vertical axis passing through the edge of the top surface of the low voltage gate insulation layer is located in the first sloped region.

In re claim 32, as far as understood, Kim shows (fig. 32) that the low voltage gate insulation layer is formed on an upper corner of the first trench region.

In re claim 33, Kim shows (fig. 32) a low voltage gate electrode (FG) formed on the low voltage gate insulation layer and disposed to cross over the first active region', and a high voltage gate electrode (313a) formed on the high voltage gate insulation layer and disposed to cross over the second active region.

In re claims 34 and 35, Kim discloses (col. 2, lines 44-50) that the low voltage region is a memory cell region. Kim shows in (fig. 31b) that the low voltage gate insulation layer is a tunnel oxide layer. 36. The semiconductor device of claim 35, further comprising: a control gate electrode formed over the tunnel oxide layer and disposed to cross over the first active region; a floating gate interposed between the control gate electrode and the tunnel oxide layer; an inter-gate dielectric layer interposed between the floating gate and the control gate electrode; a main gate electrode formed on the high voltage gate insulation layer and disposed to cross over

the second active region', and a dummy gate electrode stacked on the main gate electrode.

In re claim 36, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the second active region; a dummy gate electrode (317a) stacked on the main gate electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figure 3 (APAF) in view of Kim et al. (US 6,642,105 B2).

In re claim 22, the APAF 3 shows a semiconductor device, comprising: a semiconductor substrate having a low voltage region (A) and a high voltage region (B); a first isolation layer (11a) formed in the low voltage region and defining a first active region (7a); a second isolation layer (11b) formed in the high voltage region and

defining a second active region (7b); a low voltage gate insulation (17) layer formed on the first active region; and a high voltage gate insulation layer (15) formed on the second active region and having a greater thickness than the low voltage gate insulation layer. A step region between the high voltage gate insulation layer and the second isolation layer has a profile that is spaced apart from a vertical axis passing through an edge corner of the second active region toward the second active region toward the second isolation layer adjacent to the vertical axis. The APAF shows all of the elements of the claims except the top surface of the second isolation layer is higher than that of the high voltage gate insulation layer, without any recessed region that is lower than the top surface of the high voltage gate insulation layer. Kim et al. shows (fig. 32) a semiconductor device having a second isolation layer (309 left) that has a top surface which is higher than a high voltage gate insulation layer (305a). There are no recessed regions that are lower than that of the high voltage gate insulation layer. This configuration (col. 15, lines 20-56) prevents stringers from being formed between neighboring gate electrodes and the device performance can ultimately be improved. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the isolation layer of the APAF 3 by forming top of the isolation layer higher than the gate insulation and without a recessed region at the corners as taught by Kim to prevent stringers between neighboring gates thus improving the device performance.

In re claim 23, the APAF 3 shows a low voltage gate electrode (19) formed on the low voltage gate insulation layer, the low voltage gate electrode crossing over the

first active region; and a high voltage gate electrode formed on the high voltage gate insulation layer, the high voltage gate electrode (19) crossing over the second active region.

In re claims 24 and 25, the APAF discloses (pg. 1, lines 24-34) the low voltage region is a memory cell array region and the low voltage gate insulation layer is a tunnel oxide layer because the layer is thin and formed in the low voltage or memory cell region.

In re claim 26, as far as understood, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the second active region; a dummy gate electrode (317a) stacked on the main gate electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

In re claim 27, Kim shows (fig. 32) that a thermal oxide (311) layer is interposed between the first isolation layer (309 right) and the semiconductor substrate, and between the second isolation layer (309 left) and the semiconductor substrate.

In re claim 28, the APAF 3 shows that an edge region of the first isolation layer is lower than a top surface of the low voltage gate insulation layer because the low voltage gate insulation layer (17) is formed on top of the edge of the isolation trench.

Allowable Subject Matter

Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yeo et al. (US Pub. 2004/0129995) and Shiozawa et al. (US 6,518,635 B1) also show isolation structures for active regions wherein the structures do not have a recess region formed in the insulation profile.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
March 14, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER